Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors and overcome Examiner objections. The Examiner objects to paragraph 005, but Applicants originally Specification show this is paragraph 004; perhaps Examiner is now referring to the published version of Applicants Specification.

The claims have been amended to clarify Applicants disclosed and claimed invention and overcome Examiners objections and rejections. The amendments find support in the original claims and/or the Specification. No new matter has been added.

Claim Rejections under 35 USC 112

1. Claim 18 stands rejected under 35 USC 112, first paragraph as failing to comply with the written description requirement.

Examiner alleges that reference to "topmost metallization

layer (64) is not disclosed to be copper (Figure 2)". Examiner claims that lower part of 12 in Figure 3 "qualifies" as the claimed copper island disposed in a low dielectric material IMD "for which only 28 is a match, no etch stop layer on upper and lower main surfaces of 28 is disclosed".

Applicants respectfully suggest that Examiner is engaging in piecemeal examination by now newly erroneously misinterpreting Applicants disclosure as referring only in isolation to Figure 3 where the individual dielectric layers shown in Figure 2 making up damascene structures are not shown in Figure 3 and are generally referred to as dielectric 28. For example, one of ordinary skill would understand that damascene structures are formed in individual multiple layers of dielectrics as is generally explained in the discussion of the prior art with reference to Figure 1 at paragraph 0024:

"Fig. 1 illustrates a prior art semiconductor device 10 including a fuse 12. A layer of field oxide 14 is provided over a silicon substrate 16 including, for example, a p-well 18. Two fragments of **polysilicon** wiring 20, 22 are connected to two electrically separate devices but in a fuse arrangement, **each being upwardly connected to five levels of dual damascene structures 24, 26 that are embedded in dielectric 28**. . . As shown in Fig. 1,

a guard ring 34 is provided. This is a series of dummy dual damascene structures that form a ring completely surrounding a fuse cavity 30. The purpose is to terminate the promulgation of cracks in the dielectric 28 that may appear after the fuse 12 has been blown. While micro cracks will propagate relatively easily through the hard and brittle dielectric 28, the cracks are stopped by the soft metal of the guard ring 34."

Thus, Examiner's interpretation of Applicants disclosure with respect to claims 14 and dependent claims as referring to a different embodiment limited by Figure 3, where the individual dielectric layers for the damascene structures is not shown, while excluding the disclosure related to Figure 2, as well as the original claims, is nowhere justified by Applicants disclosure nor would be interpreted by one of ordinary skill in the art. For example see in the original claims:

"9. The semiconductor device as set forth in claim 6 wherein the structure includes a **first metal layer and a topmost metal layer** and further comprising an inter-metal dielectric layer comprising a **low dielectric constant material interposed between the first metal layer and a second metal layer of the structure.**

10. The semiconductor device as set forth in claim 9 further comprising **an etch stop layer on each face of the inter-metal dielectric layer.**"

Examiner is apparently misinterpreting Applicants independent claims e.g., 6 and 14 as referring to different embodiments included in respectively Figure 2 and Figure 3. One of ordinary skill would understand from Applicants disclosure that Figure 2 is a different and more detailed cross section and partial view of the fuse structure, whereas Figure 3 additionally shows the guard ring structure 34 surrounding the fuse structure (26, 78, 80), as shown in the prior art in Figure 1, where dual damascene structures e.g., 26 form the multi-level fuse structure, and where the individual dielectric layers necessary forming the individual levels are generally referred to as dielectric 28.

See also paragraphs 0017 and 0018 in the Specification:

Fig. 2 illustrates a semiconductor device 50 with portions broken away according to the present invention. The semiconductor device 50 may include a base portion (not shown) with discrete devices formed therein. The semiconductor device 50 may also includes an oxide or low dielectric material

52 including a number of discrete semiconductor structures (not shown) formed therein. A multilayer structure may be formed over the oxide or low dielectric material 52 including a plurality of dielectric layers 56 which may be silicon dioxide, or may be a low dielectric material such as polyimide nanoforms or porous glasses. **An etch-stop layer 54 such as silicon nitride may be positioned between adjacent layers of dielectric material.** A **damascene structure** 58 is provided in the dielectric material and includes at least a first (first from the topmost metallization layer) metallization layer 60, a plug 62 and a **topmost (second) metallization layer 64 which may be the top metallization layer.** The top metallization layer 62 may have a thickness of about 9000 angstroms or more. **A fuse 66 is formed on the topmost metallization layer 64.** Preferably the fuse is aluminum material formed at a thickness of about 1000-7000 angstroms and preferably 3500 angstroms. The fuse may be formed by an additional masking step using a patterned photoresist layer with an opening therein through which the aluminum may be deposited on top of the top metallization layer 64 by electroplating, screening or other methods known to those skilled in the art. An additional passivation layer 68 may be provided over the multilayer structures and may be a single layer or a layer of plasma enhanced silicon nitride to a thickness of about 750 angstroms and a layer of plasma enhanced oxide to a thickness of about 4000 angstroms. Additional passivation layers 72, 74 may also be provided and may be a layer of plasma enhanced oxide to a thickness of about 4000 angstroms and layer of plasma enhanced silicon nitride to a thickness of about 6000 angstroms. A fuse window 76 is provided through the passivation layers down to the fuse passivation layer 68. The fuse 66 may be blown by energizing the fuse with a laser through the fuse passivation layer 68. Preferably when the dielectric layers 52, 56 are a low dielectric material, a laser beam is utilized to blow

the fuse. The low dielectric material layers 52, 56 may have a dielectric constant k ranging from 2.0-3.6 and preferably from 2.2-3.0. **The combination of a low dielectric and a tick top metal layer such as a copper damascene structure with a low-k dielectric increases** the chance of having lower corner cracks and copper fuse residue due to the low-k dielectric softness. Lower corner cracking may produce unclean link removal and damage to the circuit. Consequently, metal links are cut more effectively at lower nominal energies and less likely to have lower corner cracking beneath the fuse link.

Fig. 3 illustrates a semiconductor device 10 having a fuse 12 according to the present invention. The structure shown in Fig. 3 is similar to the prior art structure shown in Fig. 1 **with the exception that the fuse 12 includes a first layer 78 of copper and a second layer 80 of aluminum.** Again, a thin layer of dielectric 32 overlies the fuse 12. The use of the aluminum layer 80 reduces the chance of the copper from forming oxides after the fuse is blown."

Thus, Applicants disclosure and claims make clear that:

The top metal layer (78 in Figure 3) or (64 in Figure 2) are **copper damascene structures** and that **an etch stop layer may be positioned between adjacent dielectric layers** and may be on (each face) (as claimed in original claim 10) or on an upper face and a lower face of the dielectric as disclosed. In addition, Applicants clearly show the fuse structure (item 66; Figure 2,

and item 80 in Figure 3) in alternative cross sectional views.

Thus, Applicants respectfully suggest that Examiner is now newly misinterpreting Applicants claims, thereby engaging in piecemeal examination that is contrary to Applicants disclosure as would be readily appreciated by one of ordinary skill in the art.

Examiner has not shown or explained how or why one of ordinary skill in the art would not appreciate that Applicants had possession of their disclosed and claimed invention, e.g., **including an aluminum fuse formed on copper damascene structures** (as partially shown in Figure 2 and more fully in Figure 3 including a guard ring) where "an etch stop layer on an upper main face and a lower main face of the inter-metal dielectric layer" (see item 54 in Figure 2).

Applicants respectfully refer Examiner to portions of the MPEP:

> "[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to

draw therefrom." *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968)

It is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification.

See MPEP, 8th Ed, Section 2163 (I)

An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations **using such descriptive means as words, structures, figures, diagrams**, and formulas that fully set forth the claimed invention. *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997).

While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure.

See MPEP, 8th Ed, Section 2163 (I) (B)

The fundamental factual inquiry **is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed.** See, e.g., *Vas-Cath, Inc.*, 935 F.2d at 1563-64, 19 USPQ2d at 1117.

Possession may be shown in many ways. For example, possession may be shown by describing an actual reduction to practice of the claimed invention. Possession may also be **shown by a clear depiction of the invention in detailed drawings** or in structural chemical formulas which permit a person skilled in the art to clearly recognize that applicant had possession of the claimed invention. **An adequate written description of the invention may be shown by any description of sufficient, relevant, identifying characteristics so**

long as a person skilled in the art would recognize that the inventor had possession of the claimed invention. See, e.g., *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323, 56 USPQ2d 1481, 1483 (Fed. Cir. 2000).

Thus, Applicants have clearly described their invention such that one of ordinary skill would understand that Applicants had possession of the claimed invention including the terminology in 18 (depnding from claims 17 and 14):

"The semiconductor device as set forth in claim 17 further comprising an etch stop layer on an upper main face and a lower main face of the inter-metal dielectric layer."

Thus, Examiner has failed to make out a *prima facie* case that Applicants claim language in claim 18 violates the written description requirement.

"we are of the opinion that the PTO has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims", *In Re Wertheim, 541 F.2d 257, 263, 191 USPQ 90, 97 (CCPA 1976).*

See also MPEP 2163.04(I):

> In rejecting a claim, the examiner must set forth express findings of fact which support the lack of written description conclusion (see MPEP § 2163 for examination guidelines pertaining to the written description requirement). These findings should:
> (A) Identify the claim limitation at issue; and
>
> (B) **Establish a *prima facie* case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed.**

2. Claims 19 and 21 stand rejected under 35 USC 112, first paragraph as failing to comply with the written description requirement.

Again Examiner asserts without explaining how or why one of ordinary skill would not understand that Applicants have disclosed and claimed a dielectric layer on a passivation layer since it is not disclosed in Figure 3, but is disclosed in Figure 2. Again Examiner misinterprets Applicants disclosure and asserts that Applicants has only disclosed a "copper island" in the context of Figure 3, where item 78 is clearly shown as a topmost metal line of a multi-level dual damascene structure

(e.g., 26).

Applicants respectfully suggest Examiner is now attempting to limit Applicants disclosed fused structure as claimed in claim 14 and dependent claims to Figure 3. Again, the top metal layer (78 in Figure 3) or (64 in Figure 2) are disclosed to be **copper damascene structures** and Applicants clearly show the fuse structure (item 66; Figure 2, and item 80 in Figure 3) in alternative cross sectional views.

Applicants reiterate all of the comments made above with respect to Section 112, first paragraph made with respect to claim 18 and again assert Examiner has not delineated why or how one of ordinary skill would not recognize what Applicants have disclosed and claimed and therefore, Examiner has not made out a *prima facie* case.

Nevertheless, in an effort to further Examination on the merits, Applicants have changed "copper island" to "copper damascene" in independent claim 14 as clearly outlined in Applicants disclosure.

Premature Finality

Applicants respectfully request Examiner to WITHDRAW THE FINALITY OF THE ACTION. Applicants' note that Examiner has made final the most recent office action on new grounds relying on prior art not cited by Examiner in PTO 892, paper #1, but on a commonly owned reference disclosed and discussed by Applicants **in the originally filed Applicants in the background of the invention**, e.g., Huang et al.

In addition, Examiner has made new grounds of rejection based on cited art not of record, Omura et al. (US 2004/0012073), and newly applied to independent claim 14.

Examiner has additionally cited new art not previously of record in rejecting Applicants new claims 28, which merely incorporated limitations previously claimed, i.e., Castegnetti et al.

Examiner nowhere states that Applicant's previous amendments necessitated Examiners new grounds of rejection nor required the newly cited art (see MPEP 706.07(a)), as all amendments included limitations present in previously presented claims. Indeed,

Applicants previous amendments were aimed at improving the claim language and to incorporate limitations in dependent claims to more clearly claim Applicants invention.

Applicants reproduce relevant portions of the MPEP concerning FINALITY OF OFFICE ACTIONS:

> **706.07 Final Rejection**
>
> Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, **the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied; and in reply to this action the applicant should amend with a view to avoiding all the grounds of rejection and objection.**
>
> The applicant who is seeking to define his or her invention in claims that will give him or her the patent protection to which he or she is justly entitled should receive the cooperation of the examiner to that end, **and not be prematurely cut off in the prosecution of his or her application.**
>
> **706.07(a) Final Rejection, When Proper on Second Action**
>
> Under present practice, second or any subsequent actions on the merits shall be final, except where the

> examiner **introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p).** Where information is submitted
>
> A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings **should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed.** See MPEP § 904 *et seq.* For example, one would reasonably expect that a rejection under 35 U.S.C. 112 for the reason of incompleteness would be replied to by an amendment supplying the omitted element.

Moreover, Applicants amendments included no new subject matter that was not previously claimed and where most of the amendments involved grammatical and claim style changes, as well as incorporating limitations from originally presented claims. Indeed, some of the amendments were made in response to Examiners suggestions (e.g., claim 10.

Applicants therefore, respectfully request Examiner withdraw the Finality of the most recent action to give Applicants a fair opportunity to distinguish their invention over the newly cited art, as they are entitled to do.

Claim Rejections under 35 USC 103

1. Claims 1-5 stand rejected under 35 USC Section 103(a) as being unpatentable over Kagiwata (US 6,433,406) in view of Huang et al. (6,121,073) (discussed by Applicants in the background of the Invention).

Kagiwata discloses a fuse structure and a method for manufacturing the same, where fuse elements are formed on a first insulating layer and **a portion of the first insulating layer is removed on either side of the fuse elements** (between fuse elements) **to form grooves between the fuse elements** extending **to a level below the bottom level of the fuse elements**, and forming a second insulating layer disclosed to be silicon nitride or oxide/silicon nitride which covers the sides and upper surfaces of the fuse elements and the inner surface of the grooves (see Abstract; Figures 4A-4B; col 4, lines 1-8; lines 17-30; col 5, lines 64- col 6, line 4; col 7, lines 37-43; col 8, lines 16-24).

Kagiwata further discloses that the fuse elements may be

made of **aluminum or copper** where each fuse element is provided with barrier films on the upper and lower layers of the fuse element (col 5, lines 52-54).

Kagiwata further discloses in the prior art a similar structure where a **silicon nitride film** (item 110 ;Figures 1B-1D, Figure 2C; item 8, Fig. 3B, 4D; col 7, lines 26-30) **is formed on the fuse elements**, and **includes a groove (item 113, Figure 2C; item 7, Figures 3B - 3D; Figures 4A and 4B)) formed between the fuse elements**.

Kagiwata teaches in all the embodiments, and in the disclosed prior art, that the **silicon nitride film is subsequently blown away by a laser to form a crater (recess) around the fuse elements**; col 1, lines 40-53; col 6, lines 39-54), where it is taught that **the silicon nitride film is critical** to appropriate operation of the fuse blowing operation.

Kagiwata does not disclose several aspects of Applicants disclosed and claimed invention including:

With respect to claim 1, Kagiwata does not disclose:

at least two **top metal lines comprising copper** in said top inter-metal dielectric layer, **each of said at least two top metal lines comprising a topmost metal layer in electrical communication with underlying copper interconnect structures extending through a plurality inter-metal dielectric layers;**

a fuse **comprising aluminum** on said top inter-metal dielectric layer, **said fuse providing electrical communication between said at least two top metal lines** by spanning a distance between said at least two top metal lines;"

For example, see Kagiwata items 106 and 107 (Figure 1B), where Kagiwata discloses an interconnected moisture proof **guard ring** structure (item 103; Figures 1C, Figure 2C, 2D) **surrounding and unconnected to the fuse structure.** The moisture proof ring structure is disclosed to be electrically connected through wiring (metal) layers (see col 1, lines 54-60;) **but is not connected to the fuse structure, but rather serves to stop moisture penetrating cracks formed after blowing the fuse.** Kagiwata specifically teaches away from using copper in the guard ring (wiring layers) (col 3, lines 39-46).

Kagiwata also discloses with respect (see Figure 3B), that the fuse (2) (copper or aluminum) is **connected to metal vias (6)** and connected to a single lower wiring layer (5) (see col 5, lines 49-63).

Kagiwata further does not disclose:

"**a protective layer on said fuse;** and

a window formed through a thickness portion of the protective layer, said window positioned over a top portion of said fuse."

Examiner contends that item 110, Figure 1B is equivalents to Applicants disclosed and claimed window "**as defined with indentations marking its frame as shown in Figure 1B,** said window extending through a thickness of silicon dioxide layer 109 (portion on said fuse; Figure 1B; col 3, lines 35-36)". Applicants respectfully point out that col 3, lines 35-36 are referring to grooves (item 113; Figures 2C, 2D) formed **on either side of the fuse structure** (see col 2, lines 52-54). Moreover,

the indentations shown in the Figures appear to be surface morphology effects caused by coating processes. Nowhere does Kagiwata disclose or teach any process for forming a window over the fuse structure as Applicants have disclosed and claimed by Applicants, but rather **only teaches forming groves on either side of the fuses.**

On the other hand, Huang et al. disclose an entirely different fuse structure and fuse material **(polysilicon)** (see item 14, Figure 3) which **provides the first level of electrical interconnects** i.e., formed **on field isolation regions (FOX) on the semiconductor substrate** (see col 5, lines 20-25). After forming multiple levels of metal interconnect structures of an **aluminum/copper alloy** (e.g., col 6, lines 9-10), a window opening is etched through the thickness of the **several overlying metallization layers** down to a polysilicon etch stop layer (see item 18, Figures 2, and Figure 4), the polysilicon layer is then etched through to a dielectric layer 16 overlying the **polysilicon fuse** (item 14) to provide an optical window (see col 7, lines 3-line 52).

There is no apparent motivation for combining the teachings

of Kagiwata who discloses a **copper or aluminum fuse structure** formed on top of (in electrical connection with) metal interconnect structures (metal not identified) where **grooves are formed on either side of the fuse elements** with that of Huang et al. who teach forming a **polysilicon fuse on the FOX region** of a semiconductor substrate **to form the first level of electrical interconnects**, and where an overlying window (opening) is formed extending through a thickness of several overlying metallization layers (**and where none of the metal interconnect structures is connected to the fuse**).

Moreover, any modification of Huang et al., in an effort to achieve Applicants disclosed and claimed invention would change the principle of operation of the polysilicon fuse of Huang et al. (i.e., connecting the fuse to metal lines) and make it unsuitable for its intended purpose.

Nevertheless, even assuming arguendo, a proper motivation for combining the teachings of Kagiwata and Huang et al., such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)*.

Moreover, neither Kagiwata nor Huang et al. have recognized or provided a solution to the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A semiconductor device fuse structure to prevent dielectric layer cracking at corner portions of associated metallization structures"

"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once

the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969).

Since Kagiwata in combination with Huang et al. fail to disclose the elements of Applicant disclosed and claimed invention claim, and therefore make out a *prima facie* case of obviousness, neither has a *prima facie* case been made out with respect to Applicants dependent claims.

2. Claims 6, 9, and 11 stand rejected under 35 USC Section 102(b) as being unpatentable over Kagiwata in view of Huang et al, above, and further in view of Kajita et al. (JPO020011093981 A)).

Applicants reiterate the comments made above with respect to Kagiwata and Huang et al.

Applicants reiterate that Kagiwata in combination with Huang et al. does not disclose Applicants disclosed and claimed structure:

"A semiconductor device fuse structure to prevent low dielectric material layer cracking at corner portions of associated metallization structures comprising:

two separated and respectively interconnected metallization structures, **each of said metallization structures comprising copper and extending through a plurality of low dielectric material inter-metal dielectric layers;**

wherein a fuse comprising aluminum **extends between and electrically interconnects** each of the metallization structures in an uppermost inter-metal dielectric layer; and,

a window is disposed over a top portion of said fuse, said window extending through a thickness portion of a silicon dioxide layer on said fuse."

Examiner has provided an English Abstract of Kajita et al. to Applicants. Kajita et al. teach using copper wiring in a redundancy circuit where the fuse is formed of Aluminum or an alloy of Aluminum (Al), since Al (or alloy) has a smaller

diffusion coefficient than copper, thereby preventing splashed fuse material "from diffusing **[up] to transistors formed on a silicon substrate**" (see Solution). Kajita et al. teach nothing concerning the structure of the redundancy circuit or the fuse structure.

Even assuming *arguendo* a motive for combination, the teachings of Kajita et al., in combination with Kagiwata and Huang et al., does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claim 10 stands rejected under 35 USC 103(a) as being unpatentable over Kagiwata, in view of Huang et al, further in view of Kajita et al., above, and further in view of Ying et al. (6,300,252).

Applicants reiterate the comments made above with respect to Kagiwata, Huang et al, above, and Kajita et al.

Even assuming *arguendo* a proper motivation for combination, the fact that Ying et al. (commonly owned) teach use of a silicon nitride layer (which Examiner has termed synonymous with an etch stop layer) in relation to a completely different fuse structure and metallization structures (similar to Huang et al.) where the **fuse is formed on field oxide regions on a semiconductor substrate** and **where the fuse is not connected to the metallization structures**, and further teach method for etching a fuse window through multiple overlying dielectric layers **between metal interconnect structures**, over the fuse structure, does not further help Examiner in making out a *prima facie* case of obviousness or producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

4. Claim 12 stands rejected under 35 USC 103(a) as being unpatentable over Kagiwata, in view of Huang et al, further view of Kajita et al., and further in view of Applicants alleged admitted prior art.

Applicants reiterate the comments made above with respect to Kagiwata, Huang et al, and Kajita et al.

Even assuming *arguendo* a proper motivation for combination, the fact that Applicants disclose a range of thicknesses for a fuse for such materials as platinum silicide, tantalum tungsten, or polysilicon does not further help Examiner in producing Applicants disclosed and claimed invention or making

out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claim 13 stands rejected under 35 USC 103(a) as being unpatentable over Kagiwata, in view of Huang et al, further view of Kajita et al., above, and further in view of Liaw (6,255,715).

Applicants reiterate the comments made above with respect to Kagiwata, Huang et al, and Kajita et al.

Even assuming *arguendo* a proper motivation for combination, the fact that Liaw discloses a guard ring in an unrelated fuse structure does not further help Examiner in making out a *prima facie* case of obviousness. It is noted that Applicants have also shown a guard ring structure in the prior art.

"Finally, the prior art reference (or references when

combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

6. Claim 14 stands rejected under 35 USC 103(a) as being unpatentable over Kajita et al. (JP0200109398) in view of Omura et al. (US 2004/0012073).

Neither Kajita et al. nor Omura, singly or in combination disclose Applicants claimed invention:

The disclosure of Kajita et al. teaches the use of an aluminum fuse (rather than copper) in an undisclosed circuit structure and an undisclosed fuse structure, where the use of aluminum rather than copper is generally taught to prevent diffusion of the copper through undisclosed material to transistor regions.

Omura et al. disclose a fuse structure where the first metal wiring level (disclosed to be copper damascene; paragraph 0047)

(item 102, Figure 1a-1c; item 12, Figure 3A-3D)) **and a fuse (also disclosed to be a copper damascene;** paragraph 0047) (item 101, Figure 1a-1c; item 11, Figure 3A-3D) are formed **at the same level** (see paragraph 11, 37). A fuse window opening (112) and a pad opening (over the wiring) are formed simultaneously (see Fig 1B) through overlying dielectric layers (103, 109) over the fuse (101) and an **aluminum pad** (106) (paragraph 49) deposited over the first metal wiring level (wiring copper damascene; i.e., not the fuse) (paragraph 37 and 38). Omura et al. disclose a method for simultaneously etching openings **over the fuse and wiring at the same level** to avoid residual film in the openings (see paragraph 40).

Omura et al. do not disclose the structure of the circuit or disclose electrical interconnection between the wiring and the fuse **formed at the same level.** Omura et al. **disclose both the fuse and wiring to be copper.**

Thus even assuming *arguendo*, a proper motivation for combining Kajita et al., where the circuit, fuse structure, and window structure are not shown, but teach **an aluminum fuse,** with the teachings of Omura et al., who teach the fuse and the wiring

at the same level and **made out of copper**, such combination does not produce Applicants disclosed and claimed invention.

Kajita in combination with Omura et al. do not disclose or suggest:

"A semiconductor device including a fuse comprising a first layer comprising a copper damascene disposed in a **low dielectric material** inter-metal dielectric layer and **a fuse layer on the first layer**, wherein the fuse layer **comprises aluminum**; and,

a fuse window disposed over said fuse layer, said fuse **window extending through a thickness portion of at least one dielectric layer overlying said fuse layer to a passivation layer on said fuse layer**."

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

7. Claim 16 stands rejected under 35 USC 103(a) as being unpatentable over Kajita et al. in view of Omura et al. above, and further in view of Ying et al.

Applicants reiterate the comments made above with respect to Kajita et al. and Omura.

Even assuming *arguendo*, a proper motivation for combination, the fact that Ying et al. (commonly owned with instant application) teach a dielectric layer overlying a completely different fuse structure (similar to Huang et al.) where the **fuse is formed on field oxide regions on a semiconductor substrate without connection to damascene structures**, does not further help Examiner in making out a *prima facie* case of obviousness or producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

10. Claims 17 and 20 stand rejected under 35 USC 103(a) as being unpatentable over Kajita et al. in view of Omura et al. above, and further in view of Shimooka et al. (JP 11224900).

Applicants reiterate the comments made above with respect to Kajita et al. and Omura et al., above.

Even assuming *arguendo* a proper motivation for combination, the fact that Shimooka et al. teaches multi-layered copper dual damascene wiring in an unrelated structure does not further help Examiner in making out a *prima facie* case of obviousness or producing Applicants disclosed and claimed invention.

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination". Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

11. Claims 22-26 stand rejected under 35 USC 103(a) as being unpatentable over Kagiwata, and Huang et al. as applied to claim 1, and further in view of Kajita et al., above and Pricer et al. (6,335, 229).

Applicants reiterate the comments made above with respect to and Kagiwata, Huang et al, and Kajita et al.

As noted above, the above combined references do not teach Applicants disclosed and claimed invention, therefore, the fact the Pricer discloses directing a laser beam on a completely different fuse structure (inductive loop fuse structure) where overlying dielectric layers **are first removed by laser ablation** (or etching) **prior to wet etching the fuse material** to blow the fuse (disclosed to be copper) does not further help Examiner in establishing a prima facie case of obviousness.

Moreover, there is no apparent motivation to combine the teachings of Kagiwata, who do not disclose a wavelength range, and disclose the criticality of a silicon nitride layer over the fuse for proper heating (layer 10b over a silicon oxide layer 10a) through which the laser penetrates and heats up to blow the

fuse, with the teachings of Pricer who disclose penetrating (ablating) an overlying dielectric layer and wet etching the fuse material to blow the fuse.

Nevertheless, even assuming arguendo, a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

12. Claim 28 stands rejected under 35 USC 103(a) as being unpatentable over Castegnetti et al. (6, 828,653) in view of Pricer (6,335,229).

Applicants reiterate the comments made above with respect to Pricer.

Castegnetti et al. disclose forming a fuse structure by **patterning a deposited conductive metal layer** (see Abstract)

Castegnetti et al. discloses a **damascene copper fuse** (item 109; Fig 1; item 212 Fig 2A-2C) and **damascene copper interconnect** (wiring) (item 104 Fig 1; items 211,204 Fig 2A-2C)) that are **formed on the same level** (col 2, line 60 - co 3, line 7; col 3, lines 43-47; col 5, lines 37-54). Castegnetti et al. discloses forming redistribution copper lines (211; Fig 2A-2C) over the fuse structure (212).

Castegnetti et al. the disclose forming a passivation layer (22; Fig 2A) followed by formation of an etchable metal (i.e., Aluminum) which is then patterned and etched to **form a second fuse structure** (item 236; Fig 2D; col 6, lines 44-48), followed by formation of a second passivation layer (item 238) on the **etched fuse structure**.

Thus, Castegnetti et al. does not disclose several aspects of Applicants disclosed and claimed invention:

A method of blowing a fuse structure to prevent low

dielectric material layer cracking at corner portions of associated metallization structures, said fuse structure comprising:

a **fuse window formed through at least one dielectric layer** overlying an upper face of an aluminum fuse **to expose a passivation layer** comprising silicon dioxide on said fuse, said fuse window selectively disposed over said upper face of said aluminum fuse;

said aluminum fuse spanning a distance between two copper metallization structures, **each of said copper metallization structures comprising interconnected damascene structures extending through a plurality of low dielectric material layers;**

wherein said method comprises:

directing a laser beam **onto said fuse through said silicon dioxide passivation layer** using a wavelength ranging from 300-500 or 1000-1400 nm.

Thus, even assuming arguendo, a proper motivation for

combination, such combination does not produce Applicants disclosed and claimed invention.

Nowhere do Castegnetti et al. disclose Applicants disclosed and claimed fuse structure, or a method for blowing the same.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

None of the multiplicity or cited references, including newly cited references, singly or in combination, disclose or suggest Applicants disclosed and claimed invention, nor provide Applicants solution to the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A semiconductor device fuse structure to prevent dielectric layer cracking at corner portions of associated metallization

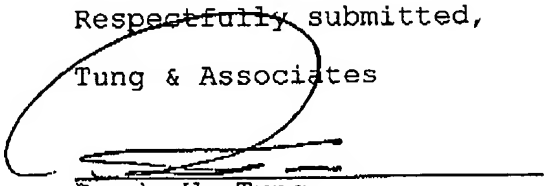
structures"

Based on the foregoing, Applicants respectfully request reconsideration of their claims and submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates



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